

**DEPT. of Computer Science Engineering**

**SRM IST, Kattankulathur – 603 203**

**Sub Code & Name: 18CSS201J - ANALOG AND DIGITAL ELECTRONICS**

|  |  |
| --- | --- |
| **Experiment No** | **07** |
| **Title of Experiment** | **Design and implementation of 2 bit comparator** |
| **Name of the candidate** |  |
| **Register Number** |  |
| **Date of Experiment** |  |

**Mark Split Up**

|  |  |  |  |
| --- | --- | --- | --- |
| **S.No** | **Description** | **Maximum Mark** | **Mark Obtained** |
| 1 | Oral Viva / Online Quiz | 5 |  |
| 2 | Circuit Connection and Execution | 10 |  |
| 3 | Verification of truth table | 5 |  |
| **Total** | | **20** |  |

**Staff Signature with date**

**7. a. Design and implementation of Magnitude Comparator Combinational circuits using simulation package**

**Aim**

To Design a magnitude comparator using Multisim software and to verify its truth table.

**Apparatus / Software Required:**

MULTISIM SOFTWARE

### Theory:

A magnitude digital comparator is a combinational circuit that compares two digital or binary numbers in order to find out whether one binary number is equal, less than or greater than the other binary number. We logically design a circuit for which we will have two inputs one for A and other for B and have three output terminals, one for A > B condition, one for A = B condition and one for A < B condition.

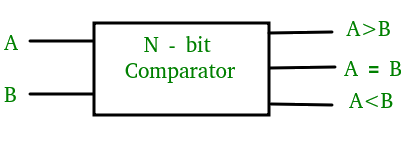


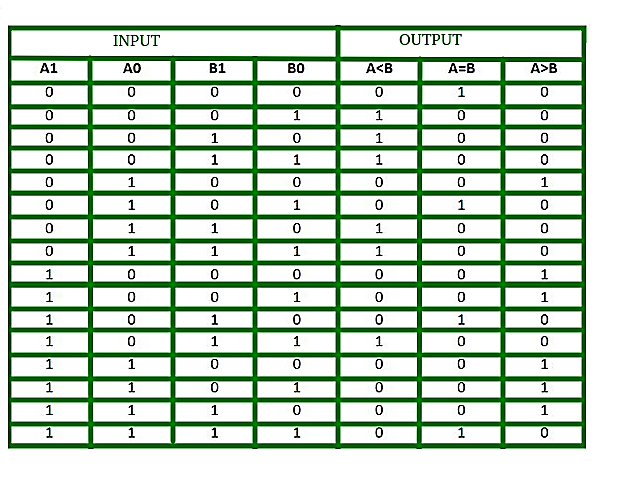
Figure-1: Block Diagram of Comparator

### 2-Bit Magnitude Comparator:

A comparator used to compare two binary numbers each of two bits is called a 2-bit magnitude comparator. It consists of four inputs and three outputs to generate less than, equal to and greater than between two binary numbers.

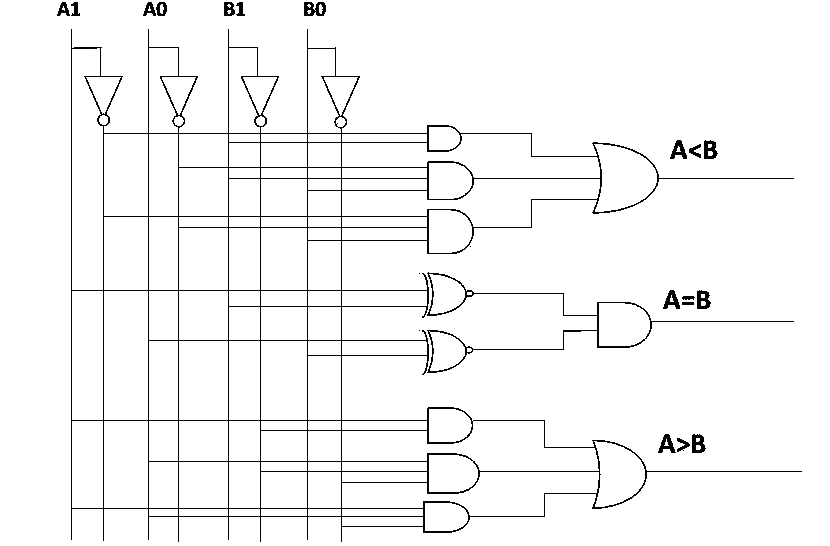
**Truth Table:**

The truth table for a 2-bit comparator is given below:

  
Figure-2: Truth Table of 2-Bit Comparator

The logical expressions for each output can be expressed as follows:  
A > B : A1B1’ + A0B1’B0’ + A1A0B0’  
A = B : A1’A0’B1’B0’ + A1’A0B1’B0 + A1A0B1B0 + A1A0’B1B0’  
           : A1’B1’ (A0’B0’ + A0B0) + A1B1 (A0B0 + A0’B0’)  
           : (A0B0 + A0’B0’) (A1B1 + A1’B1’)  
           : (A0 Ex-Nor B0) (A1 Ex-Nor B1)  
A < B : A1’B1 + A0’B1B0 + A1’A0’B0

**Logical Diagram:**

  
Figure-3: Logic Circuit of 2-Bit Magnitude Comparator

Multisim Diagram:

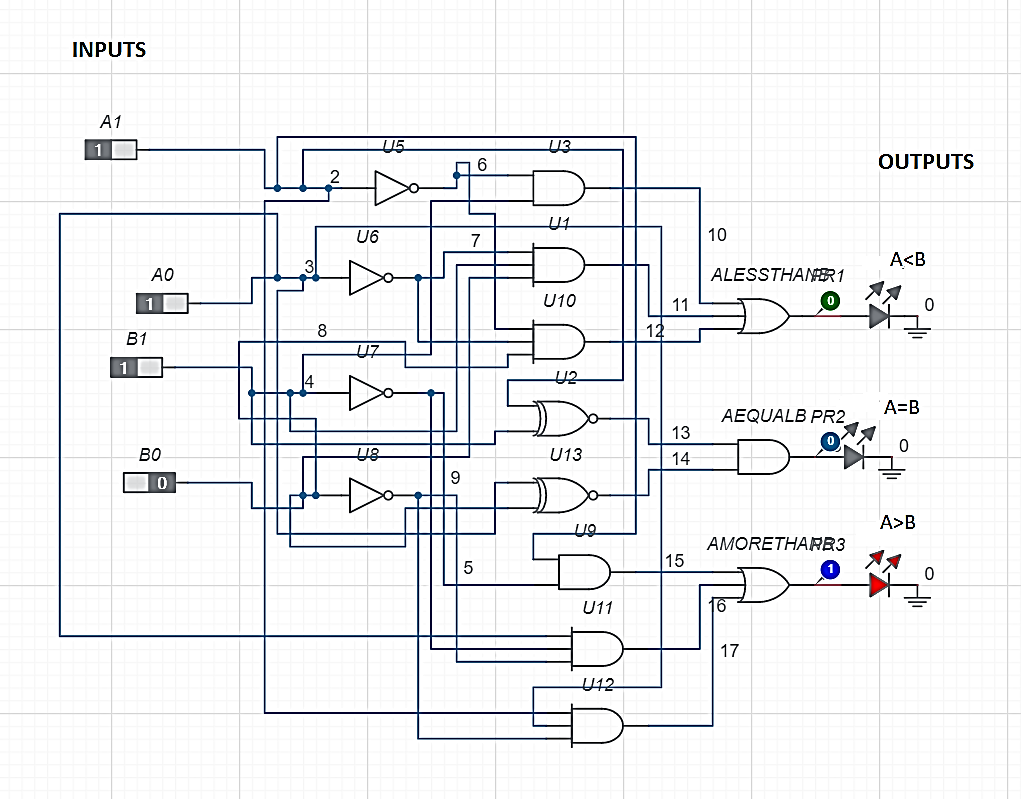


Figure-4: Multisim Circuit of 2-Bit Magnitude Comparator

**Simulation diagram:**

**Input:**

**Output:**

**Result:**

Thus the 2 bit magnitude comparator was designed and verified with the truth table using Multisim software.

**Expt No: 7b**

**Date:**

**Hardware Implementation Using Virtual Laboratory**

**Aim**

1: To Design a magnitude comparator using virtual laboratory platform and to verify its truth table,

**Apparatus / Software Required:**

Virtual Laboratory (Link)

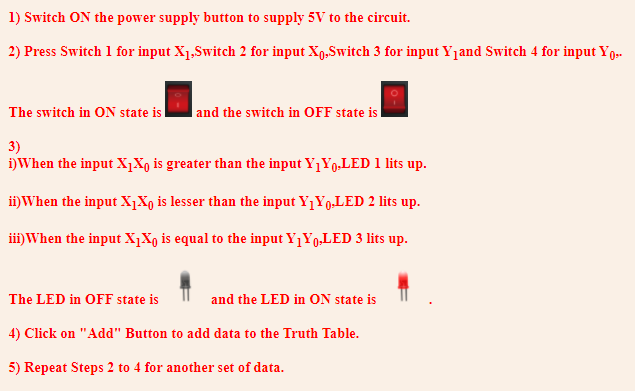
<http://de-iitr.vlabs.ac.in/digital-electronics-iitr/exp/comparator-using-logic-gates/round-template/experiment/simulation/comparator/2%20BIT%20COMPARATOR/Simulator.html>

**Theory:**

A comparator used to compare two binary numbers each of two bits is called a 2-bit Magnitude comparator. It consists of four inputs and three outputs to generate less than, equal to and greater than between two binary numbers.

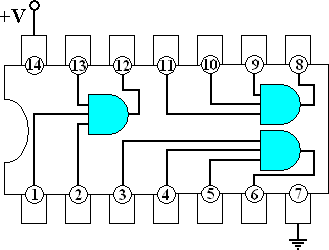
**i. Simulator 1: Construction of 2-Bit Comparator using ICs**

**Procedure:**

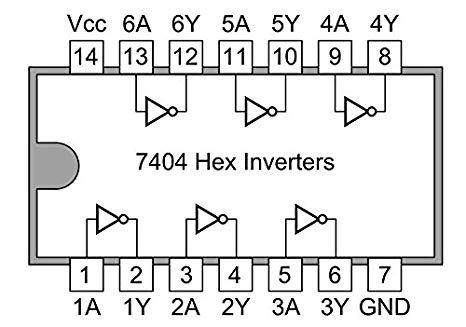


**IC Details:**

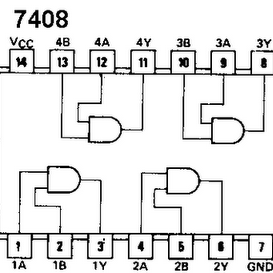
1. **IC 7411**



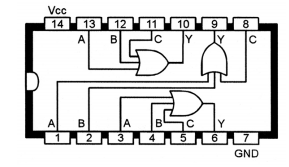
1. **IC 7404**



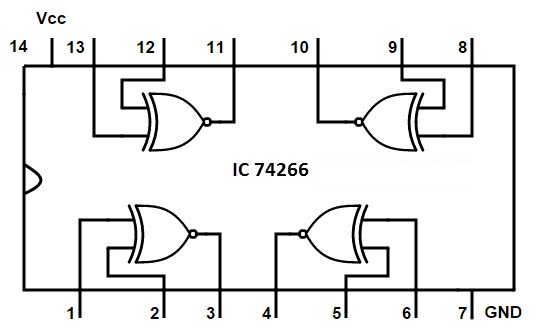
1. **IC 7408**



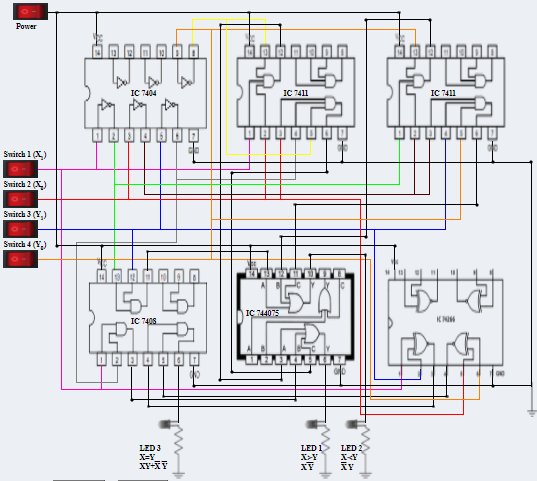
1. **IC 744075**

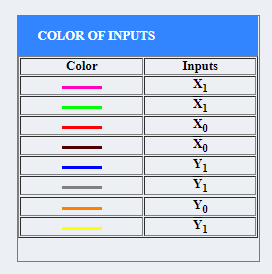


1. **IC 74266**

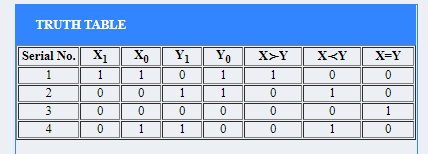


**Circuit Diagram:**

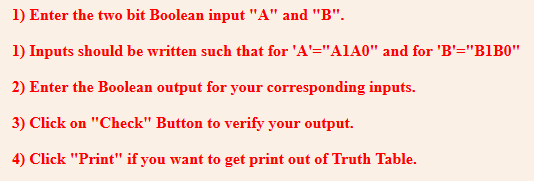


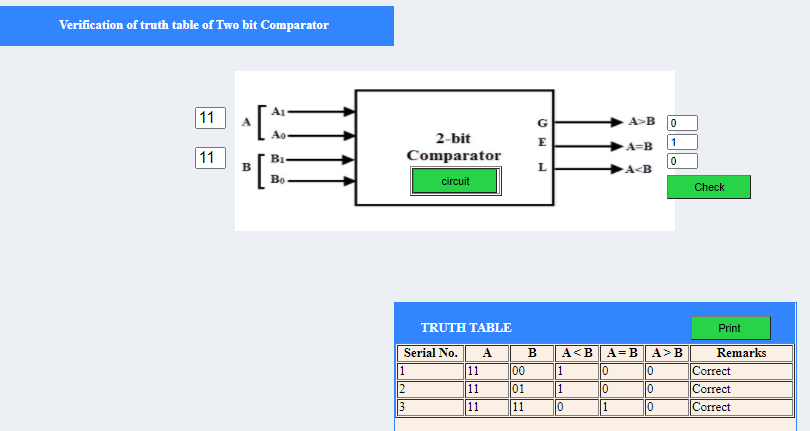


**Sample verification table:**



**ii) Simulator 2 - Verification of truth table of Two bit Comparator**

**Procedure:** 



**Simulator 1 Truth table:**

**Simulator 2 Truth table:**

**Result:**

Thus the 2 bit magnitude comparator was designed and verified with the truth table using Virtual Lab.